A 14-Bit ADC that is Both Fast and Low Noise

by Richard Reay and Dave Thomas

Introduction

The LTC1744 is an exception to the rule that an ADC must tradeoff low noise performance for high sampling rates. The LTC1744 is a 14-bit ADC that has excellent dynamics and linearity at sampling rates up to 50Msps, making it ideal for communications, scanners and high-speed data acquisition. Pin selectable input ranges of $2V_{P-P}$ and $3.2V_{P-P}$ along with a resistor programmable mode allow the LTC1744's input range to be optimized for a wide variety of applications. Its low jitter of 0.3ps allows undersampling of IF frequencies of up to 70MHz and beyond with excellent noise performance.

The LTC1743 is a pin compatible 12-bit part.

LTC1744 Features

- 50Msps sample rate
- 77dB SNR and 87dB SFDR at 5MHz input
- 150MHz full power bandwidth sampling
- $2V_{P-P}$ to $3.2V_{P-P}$ input range
- 0.5V to 5V digital output range
- 48-pin TSSOP package

Flexible, Yet Easy to Use

The LTC1744 is a complete solution with an on-chip sample and hold, a 14-bit pipelined ADC and a 30ppm programmable reference, as shown in block diagram in Figure 1. The wide-band sample and hold circuit can sample analog inputs beyond the Nyquist rate up to its 150MHz bandwidth. There is a low impedance, 2.5V reference output provided (V_{CM}) that can be used to set the common mode voltage of the analog inputs. The on-chip programmable reference can be set for a $2V_{P-P}$ or $3.2V_{P-P}$ input range, or any range in between by using two external resistors.

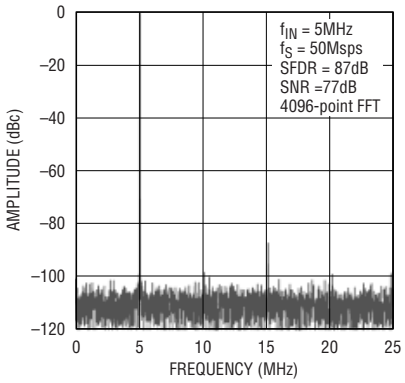

Figure 2. FFT with a 5MHz input signal

At 77dB SNR, the LTC1744 has the lowest noise of any ADC at this speed. The distortion performance of the LTC1744 is exceptional, with typical values of 87dB SFDR for a 5MHz input signal, and 73dB SFDR for a 70MHz input signal. Figure 2 shows a 4096-point FFT plot of the LTC1744 with a 5MHz input signal.

continued on page 38

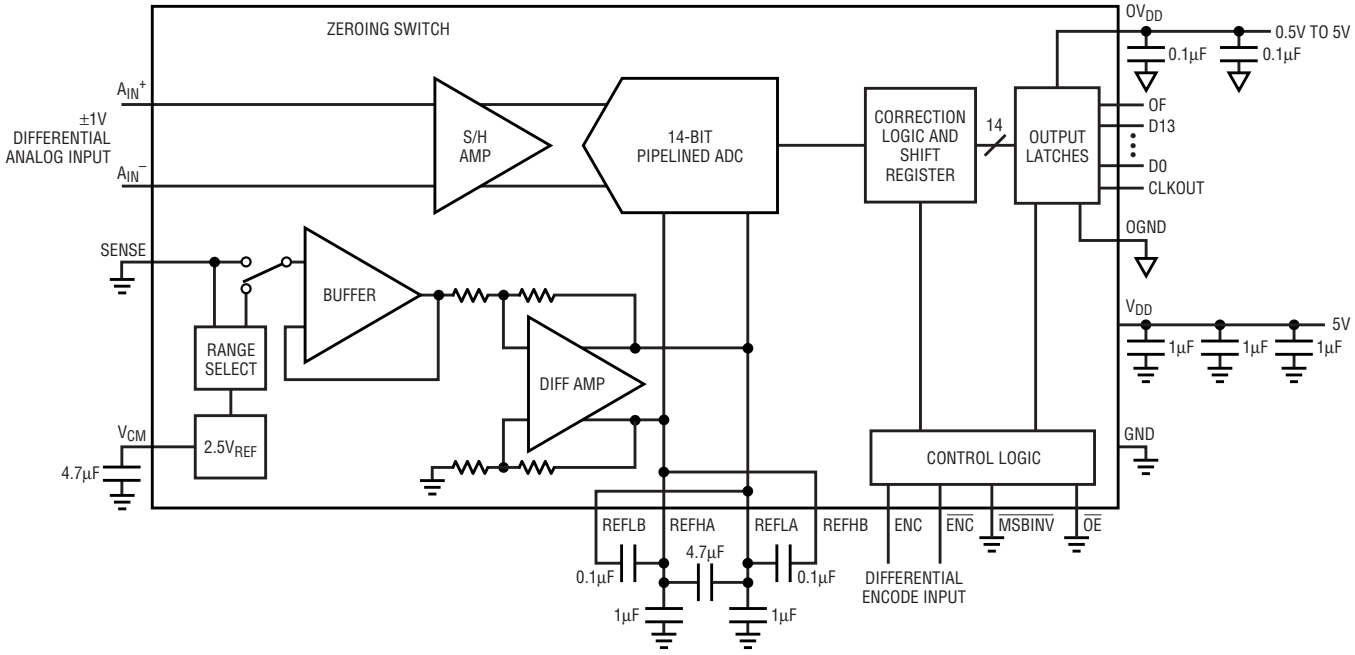

Figure 1. Block diagram

LTC1744, continued from page 33

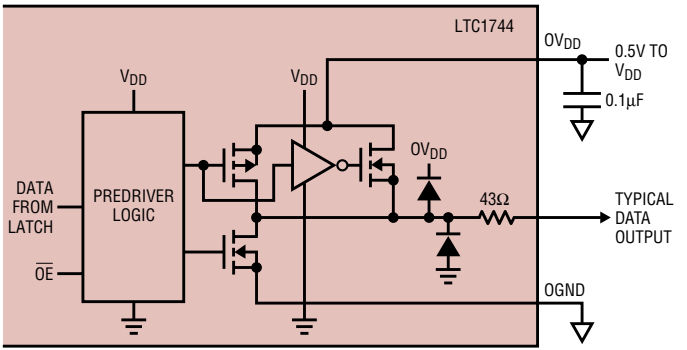

Figure 3. Equivalent circuit for a digital output buffer

Programmable On-Chip Reference

When using high-speed ADCs, there is a tradeoff between using a small input range for clean distortion performance and a larger input range for low noise. The LTC1744 gives the user the flexibility to choose the optimal input range for the application. There are two built-in input ranges that can be selected using the SENSE pin. With SENSE tied to V_{DD}, the input range is $3.2V_{P-P}$, and with SENSE tied to GND, the input range is $2V_{P-P}$. If another input range is desired, SENSE can be driven with an external reference or by a resistor divider from the on-chip 2.5V reference to generate any input range between $2V_{P-P}$ and $3.2V_{P-P}$.

Easy Interface to 5V, 3V or LVDS Systems

The LTC1744 offers flexible digital output range making it versatile and easy to use. Figure 3 shows an equivalent circuit for one of the digital output buffers. Each buffer is powered by the OV_{DD} and OGND pins, which are isolated from the ADC power and ground. The OV_{DD} supply can be set from 0.5 to 5V, allowing direct interface to any CMOS logic family, TTL or LVDS. In high speed ADCs, coupling from the digital outputs to the analog input can degrade the noise performance. Reducing the output swing minimizes this effect.

Conclusion

The LTC1744 is a flexible 14-bit 50Msps ADC that offers industry-leading low noise performance and features that make it both versatile and easy-to-use.

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